METHOD AND APPARATUS FOR OPTIMIZING BODY BIAS CONNECTIONS IN CMOS CIRCUITS USING A DEEP N-WELL GRID STRUCTURE

ABSTRACT OF THE DISCLOSURE

A method and apparatus for optimizing body bias connections to NFETs and PFETs using a deep n-well grid structure. A deep n-well is formed below the surface of a CMOS substrate supporting a plurality of NFETs and PFETs having a nominal gate length of less than 0.2 microns. The deep n-well is a grid structure with a regular array of apertures providing electrical continuity between the bottom of the substrate and the NFETs. At least some of the PFETs reside in surface n-wells that are continuous with the buried n-well grid structure. The grid and n-well layout is performed on the basis of the functionality of the PFETs contained in the n-wells.